Ben Limpanukorn

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Education

2022 – Present	Ph.D., University of California, Los Angeles (UCLA) Computer Science
2021 - 2022	M.S., University of California, Los Angeles (UCLA) in Computer Science.
	Capstone: Challenges and Methods for Testing NVMe SSD Devices using Software Fuzzing Techniques.
2017 – 2021	B.S., University of California, Los Angeles (UCLA) in Computer Science and Engineering.

Publications

Conference Proceedings

J. Clifford, **B. Limpanukorn**, and E. Jimenez, "An improved process to colorize visualizations of noisy x-ray hyperspectral computed tomography scans of similar materials.," 2022. *O* URL: https://api.semanticscholar.org/CorpusID:265029352.

J. Clifford, E. Kemp, **B. Limpanukorn**, and E. S. Jimenez, "A process to colorize and assess visualizations of noisy x-ray computed tomography hyperspectral data of materials with similar spectral signatures," 2021, pp. 1–8. *O* URL: https://api.semanticscholar.org/CorpusID: 252166322.

Experience

2020 – Present **Graduate Student Researcher** SEAL Lab at UCLA.

- Currently investigating methods to effectively fuzz test compilers by mutating inputs to satisfy automatically inferred constraints.
- Evaluated the potential uses and limitations of software fuzzing techniques for testing NVMe SSDs.

R&D Graduate Student Intern Sandia National Laboratories.

- Currently part of a team leading the development of new airport security screening workflows to improve threat detection, preserve passenger privacy, and reduce passenger wait time.
- Productionized object detection models for next-generation millimeter-wave scanners, resulting in a 6x reduction in inference time and improved precision/recall compared to a baseline model.
- Developed new methods to colorize/visualize hyperspectral CT data by combining dimension reduction (e.g. UMAP and T-SNE) with generalized linear models to improve the interpretability of spectrally similar materials.
- Used Vitis HLS to develop an FPGA implementation of a List-Mode MLEM reconstruction algorithm, achieving a 5x speed-up compared to an equivalent CPU implementation.

Experience (continued)

